REMARKS

Objection to the Drawings

The examiner objected to the drawings for purportedly not showing the passivation layer covering the flash memory cell, or the floating gate. Figure 1 shows passivation layer 103 covering semiconductor substrate 101. The specification states that semiconductor substrate 101 "includes conventional flash memory features, including flash memory cells (not shown). Each flash cell includes a floating gate . . . " (See specification at page 3, lines 20-22.) Because the drawings show passivation layer 103 covering substrate 101, which contains flash memory cells that include floating gates, it necessarily follows that the drawings represent passivation layer 103 covering the flash memory cells, which include floating gates.

The drawings do not need to provide additional detail for the flash memory cells located in substrate 101. In particular, the drawings do not need to illustrate the flash memory cells' floating gates. Flash memory cells, and flash memory cell floating gates, are conventional features of a flash memory. It is appropriate to illustrate such features schematically. In this regard, 37 C.F.R. §1.83(a) provides:

> . . . conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).

Flash memories necessarily have flash memory cells, and flash memory cells necessarily have floating gates. Figure 1 illustrates these features schematically as th y are conventional features for which a d tailed illustration is

not essential for a proper und rstanding of the invention. As the specification describes, and as figure 1 illustrates, the invention calls for forming a passivation layer from a material that is opaque to ultraviolet light, which covers conventional flash memory cells (including their floating gates) that all flash memories contain. There is no reason to include in the drawings unnecessary detail that relates to such conventional components.

Because applicants' figure 1 schematically represents a conventional flash memory structure, which necessarily includes flash memory cells and their floating gates, in precisely the manner 37 C.F.R. §1.83(a) recommends, there is no reason to modify the drawing to include additional detail. For that reason, applicants respectfully request the examiner to withdraw the objection to the drawings.

Rejection Under 35 U.S.C. §112

The examiner rejected claims 9-15 under 35 U.S.C. §112, first paragraph, for purportedly containing subject matter that was not described in the specification. Specifically, the examiner contends that the phrase "the passivation layer covering the flash memory cell" is not supported by the original disclosure. Applicants disagree.

To comply with the written description requirement, the specification need not describe the claimed subject matter in exactly the same terms as used in the claims; it must simply indicate to persons skilled in the art that as of the filing date the applicant had invented what is now claimed. The failure of the specification to specifically mention a limitation that later appears in the claims is

not a fatal one when one skill d in the art would recognize upon reading the specification that the new language reflects what the specification shows has been invented. All Dental Prodx, LLC v. Advantage Dental Prods, Inc., 309 F.3d 774 (Fed. Cir. 2002). If a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate written description requirement is met. In re Alton, 76 F.3d 1168, 1175 (Fed. Cir. 1996).

Figure 1 shows passivation layer 103 covering semiconductor substrate 101. The specification states that semiconductor substrate 101 "includes conventional flash memory features, including flash memory cells (not shown)." (See specification at page 3, lines 20-22.) Because passivation layer 103 covers substrate 101, which includes flash memory cells, it necessarily follows that passivation layer 103 covers the flash memory cells.

The specification (at page 6, line 3, through page 7, line 2) confirms that passivation layer 103 covers the flash memory cells that are included in the claimed flash memory. Here, the specification describes forming an ultraviolet ("UV") opaque passivation layer, which comprises a silicon nitride barrier layer 104 and a polyimide stress reduction layer 105. The silicon nitride layer is formed using a conventional plasma enhanced chemical vapor deposition ("PECVD") process, and the polyimide layer is spun onto the silicon nitride layer. Because such PECVD and spin-on processes deposit these materials over the

entire structure, the resulting passivation layer must necessarily cover the device's flash memory cells.

For these reasons alone, anyone skilled in the art will immediately recognize that the structure applicants described in the original specification includes a passivation layer that covers the claimed device's flash memory cells. This is even more evident given that the essence of applicants' patented process is that it permits a UV opaque passivation layer to cover the flash memory cells of a flash memory. As explained in the Background of the Invention section of the specification (page 2, lines 9-25), charge may build up on the floating gates of the flash memory cells as the device is made. Prior to applicants' invention, the device was exposed to UV radiation to neutralize that charge after the passivation layer was formed. As a result, previous flash memories could not include a UV opaque passivation layer because such a layer would prevent UV radiation from reaching the flash memory cells' floating gates. A UV opaque passivation layer would prevent UV radiation from reaching the flash memory cells because the passivation layer covered them.

To enable a flash memory to include a UV opaque passivation layer, applicants devised the process claimed in U.S. Patent No. 6,350,651. That patent issued from the parent application from which the pending divisional application claims priority. That process exposes the device to UV light to neutralize process induced charge before forming the passivation layer. This change in process sequence enables a UV opaque passivation layer to be formed – notwithstanding the fact that the passivation layer must cover the flash

memory cells. The examiner must recognize that there would not be any advantage to applicants' new process, over prior practice, unless the passivation layer in the claimed flash memory covered the flash memory cells.

Because the passivation layer in a flash memory device covers the flash memory cells, prior processes required a UV transparent passivation layer to enable UV light to reach the flash memory cells. Applicants' patented process enables a UV opaque passivation layer to be used instead, despite the fact that it covers the flash memory cells, because applicants' process exposes the device to UV light (to neutralize process induced charge) before forming the passivation layer. Anyone skilled in the art would thus appreciate, based on the basic structure of flash memories and the nature of applicants' invention, that applicants' specification must disclose a flash memory with a passivation layer that covers the flash memory cells.

For the reasons set forth above, applicants' specification adequately supports the phrase "the passivation layer covering the flash memory cell," despite not including these precise words. In this regard, applicants invite the examiner to consider In re Wright, 866 F.2d 422 (Fed. Cir. 1989). In that case, the Court of Appeals for the Federal Circuit reversed a decision from the Board of Patent Appeals and Interferences, which had upheld the rejection of an amended claim under 35 U.S.C. §112, first paragraph, based on the specification supposedly not providing an adequate written description of a particular element.

In In re Wright, the rejected claim covered a method of forming images that included depositing a layer of photosensitive microcapsules in the form of a free-flowing powder. The claim had been amended by adding a limitation, which specified that the powder be "distributed upon said support but not permanently fixed thereto." The specification, as filed, did not include the exact phrase "not permanently fixed." Nonetheless, the Court held that the original disclosure unequivocally taught the absence of permanently fixed microcapsules. The Court supported that conclusion by noting that the specification's examples indicated that the microcapsules should be distributed so as not to change their position until the image is formed by rupturing. Because those examples suggested that the microcapsules' position would be changed after the image was formed, they demonstrated that the microcapsules were not permanently fixed – as specified in the amended claim.

As in In re Wright, applicants' drawings and specification indicate that the passivation layer must cover the flash memory cells – even though the specification does not provide the precise language that was added to amended claim 9. That disclosure -- which describes applying the UV exposure step before forming the passivation layer, thereby, enabling a UV opaque passivation layer to cover the flash memory cells -- adequately supports the phrase "the passivation layer covering the flash memory cell." Accordingly, applicants respectfully request the examiner to withdraw the rejection of claims 9-15 under 35 U.S.C. §112.

Rejection Und r 35 U.S.C. §102(b)

The examiner rejected claims 9, 10 and 15 under 35 U.S.C. §102(b) as being anticipated by Shirota et al. To support that rejection, the examiner contends that Shirota's nonvolatile memory is inherently a flash memory because a flash memory is a type of nonvolatile memory device. The examiner further contends that Shirota's device includes a passivation layer that is not transparent to ultraviolet light.

Shirota does not anticipate the flash memories of claims 9, 10 and 15. Claim 9 specifies a flash memory. Applicants agree with the examiner that a flash memory is a type of nonvolatile memory device. It does not follow, however, that all nonvolatile memories are inherently flash memories, as the examiner seems to suggest. Although some nonvolatile memories (e.g., flash memories) are erased electrically, others must be erased by exposing them to UV radiation. Shirota does not describe a flash memory, which must be erased electrically, but instead describes a different type of EPROM – i.e., one that is erased using UV light. Because Shirota describes a UV erasable EPROM, but does not describe a flash memory, that reference cannot anticipate the flash memory of claim 9.

Shirota does not anticipate that claim for another reason. Claim 9 requires a passivation layer that is not transparent to UV light. Shirota's device does not include such a passivation layer. Because Shirota's memory cell mainframe is erased using UV illumination (see Shibota at column 1, lines 36-38, and at column 3, lines 17-20), Shirota's passivation film 3 must be transparent to

UV light. If Shirota's passivation film 3 was opaque to UV light, as claim 9 requires, the memory cell mainframe could not be erased by exposing it to UV light because UV light could not pass through that passivation layer.

Shirota's UV impermeable resin film, e.g., polyimide film 1, is not a passivation layer that is opaque to UV light for a different reason. Although polyimide film 1, unlike passivation film 3, is opaque to UV light, it is not a passivation layer. As Shibota itself indicates, a passivation layer serves to protect the underlying structures, e.g., the wiring pattern, from moisture and other substances that may corrode, rust, or otherwise adversely affect those structures. (See Shibota, at column 1, lines 26-29.)

Shibota's polyimide film 1 does not seal the device to protect underlying structures from exposure to corrosive materials. Polyimide film 1 instead serves to prevent UV light from reaching "special information memory cells," which include information that must not be erased, when UV light is applied to erase information contained in the memory cell mainframe. Because polyimide film 1 covers the special information cells, but does not cover the memory cell mainframe, that film cannot fill the passivation layer role. Moreover, because a polyimide film will not prevent corrosive materials from passing through it to attack the underlying structure, it cannot serve as a passivation layer for this additional reason. (Note that the polyimide layer in applicants' claimed device acts as a stress reduction layer – not as a barrier layer, a role that must be filled by another type of material, e.g., silicon nitride. Although it may be proper to charact rize the combination of silicon nitride and polyimide layers as a

passivation layer, if both layers cover the entire device, a polyimide layer alone cannot serve as a passivation layer.)

Because Shirota's passivation layer 3 must be transparent to UV light, and because Shirota's polyimide film 1 is not a passivation layer, Shirota's device lacks a passivation layer that is not transparent to UV light. For this additional reason, Shibota's device does not anticipate the flash memory of applicants' claim 9.

The claimed invention relates to flash memories, not UV erasable EPROMs. In addition, the claimed invention requires a passivation layer that is not transparent to UV light – a feature missing from Shirota's UV erasable EPROM. For these reasons, Shirota cannot anticipate the flash memory of claim 9, or the flash memories of dependent claims 10 and 15. Accordingly, applicants respectfully request the examiner to withdraw the rejection of these claims based upon Shirota allegedly anticipating them.

Rejections Under 35 U.S.C. §103(a)

The examiner rejected claim 11 under 35 U.S.C. §103(a) as being unpatentable over Shirota in view of Kiyohiko, and rejected claims 12-14 under 35 U.S.C. §103(a) as being unpatentable over Shirota in view of Kiyohiko, and further in view of Jeuch. These claims depend upon claim 9. As explained above, claim 9 specifies a flash memory that includes a UV opaque passivation layer, which covers the flash memory cell. None of the cited references describes a flash memory that includes such features. Nor do those references provid any teaching or suggestion that would have motivated one skilled in the

art to modify any of the devices they describe by incorporating into them a UV opaque passivation layer that covers a flash memory cell.

On the contrary, both Shirota and Kiyohiko teach away from including those features in such a device. Both references describe EPROMs that must be erased by exposing them to UV radiation. Shirota enables UV light to erase its memory cell mainframe by restricting polyimide film 1 to the "special information memory cells." As already explained, Shirota's passivation film 3 must be transparent to UV light to enable the memory cell mainframe to be erased. Kiyohiko teaches to form a window through the passivation layer to enable UV radiation to reach the memory cells, so that information included in them may be erased.

Shirota's and Kiyohiko's EPROMs can be erased only by exposing their memory cells to UV radiation. Modifying their devices to cause a UV opaque passivation layer to cover the memory cells would have rendered them inoperable because such a passivation layer would prevent UV radiation from reaching the memory cells. Because those skilled in the art would have recognized that covering the memory cells in Shirota's and Kiyohiko's EPROMs with a UV opaque passivation layer would yield inoperative devices, it would not have been obvious to them to modify those devices in that way.

Unlike Shirota's and Kiyohiko's UV erasable EPROMs, flash memories do not require UV exposure to erase them. For that reason, they may be erased even when their flash memory cells are covered with a UV opaque passivation layer. Notwithstanding that fact, conventional wisdom – prior to applicants'

invention – held that even flash memories could not include a UV opaque passivation layer that covers the flash memory cells. The reason why is because even these devices' memory cells required UV exposure to neutralize any electronic charge that had built up on the memory cells during the process for making the device. Because that UV exposure step was performed after the passivation layer was formed, it was not possible for the device to include a UV opaque passivation layer that covered the flash memory cells.

Applicants discovered that such a UV exposure step could effectively neutralize electric charge -- even when applied before forming the passivation layer, as long as that UV exposure step was performed after patterning the final metal layer. Not until applicants invented that now patented process was it even possible to make the flash memory of claim 9, which includes a UV opaque passivation layer that covers the flash memory cell. It logically follows that the claimed flash memory is patentable for essentially the same reasons that the process for making it is patentable – as the Patent Office previously acknowledged when issuing U.S. Patent No. 6,350,651.

For the reasons set forth above, the flash memory of claim 9 is patentable over the combination of Shirota, Kiyohiko and Jeuch. Because claims 11-14 depend upon claim 9, they are likewise patentable over the cited references. Consequently, applicants respectfully request the examiner to withdraw the rejection of these claims based on 35 U.S.C. §103(a).

The flash memories claimed in all pending claims are patentable over the cited referenc s, either when considered alone or in combination. Accordingly,

applicants respectfully request the examiner to allow pending claims 9-15 to issue.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION
(37 C.F.R. § 1.8(a))

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